EVALUATION OF SiC GTOs FOR PULSE POWER SWITCHING

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Abstract

Certain applications require devices that can switch high peak current with fast rise times and narrow pulse width. This work was done as an initial study to investigate the performance of Silicon Carbide (SiC) Gate turn-off thyristor (GTO) in these applications. The SiC GTOs were designed for high turn-off gain and not optimized for pulse applications. The GTOs were tested as discharge switches in a low inductance circuit delivering 2μs pulses with a maximum switching current of 1.4 kA (94.6 kA/cm^2) and a current rise time of 2.4 kA/μs. All the devices were switched until failure. The failure modes will be discussed.

I. INTRODUCTION

The demand for smaller and higher power density power electronics and pulse power systems requires that the semiconductor switches operate at higher switching frequency and at higher temperature. Because the new requirements are pushing the limit of current Silicon (Si) power semiconductors, new materials such as SiC are being investigated for power devices. The advantages of SiC power devices over Si devices are faster switching speed, higher operating temperature, and higher blocking voltages. The improved performance of SiC devices over Si is attributed to the unique properties of SiC material [1]. These improvements include wide bandgap (3.2 eV for 4H-SiC), high electric breakdown strength (2.2 MV/cm) and high thermal conductivity (~3 W/cm·K) [2]. Researchers have characterized SiC devices for high temperature and high-voltage applications switching into an inductive load [3]. For pulse power applications, semiconductor devices are stressed at a higher peak current and a faster current rise time than in the continuous power electronics applications. High peak current and fast rise time can cause localized heating in the device, which can lead to thermal runaway and failure of the devices [4]. This work was provided as an initial investigation onto the ability of SiC devices to operate at extremely high pulse power density for Army lethality and survivability systems. The failure of the devices while operating at high peak currents and fast rise times is investigated. The Scanning Electron Microscope (SEM) is used to evaluate the failure in the devices and the results are discussed. The results from this work will help in design and development of future SiC devices for pulse power applications.

II. EXPERIMENTAL PROCEDURE AND SYSTEM

A. Device

The following discussion gives the details of the device under test. An idealized cross section of the 4 mm^2 (anode mesa area) GTO is given in figure 1. This device was designed and fabricated by CREE Inc. to provide ≈ 1200 V forward blocking voltage and a maximum controllable current density of 500 A/cm^2 (or ≈7 A based on an active area of 37% of the total mesa area). As these devices are asymmetric, their reverse blocking voltage is limited to ≈250 V. The junction termination extension (JTE) reduces the electric field crowding at the edges of the junction, J_2, thereby increasing the forward blocking voltage [5]. Note that the control signal for this structure is applied between the gate and anode — unlike many conventional silicon GTOs. A detailed description of the CREE GTO can be found in Reference [6]. The SiC GTOs are capable of operating at case temperature up to 150 ^{0}C as presented in references [7, 8].

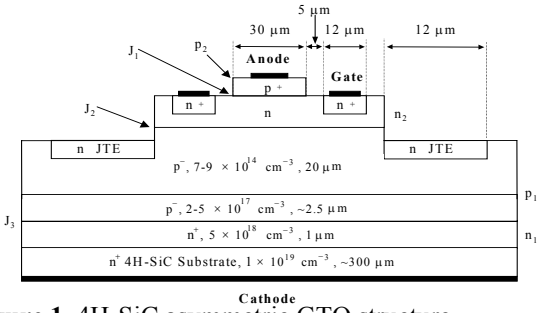

Figure 1. 4H-SiC asymmetric GTO structure

B. Circuit

A ring down RLC circuit as shown in figure 2 was used for this experiment. The capacitor C was charged up through the charging resistor R_C. The GTO is used to discharge the capacitor into the load resistor R_L. A load resistance of 0.25 ohms was used. Figure 3 and figure 4 shows the front and backsides of the complete circuit respectively. The switching circuit was designed in a compact wagon wheel configuration to minimize the stray inductance. The resistors were mounted on the front and the capacitors were connected to the back of the fixture. The circuit, when charged up to 700 V, will produce a peak current of 1.4 kA with a full pulse width of 2 μs. The di/dt, which, is defined as the time it takes the current to rise from 10% to 90% of the peak current was designed for 3.5 kA/μs. In order to achieve fast current rise time, the inductance in the system must be minimized. The

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14. ABSTRACT
Certain applications require devices that can switch high peak current with fast rise times and narrow pulse width. This work was done as an initial study to investigate the performance of Silicon Carbide (SiC) Gate turn-off thyristor (GTO) in these applications. The SiC GTOs were designed for high turn-off gain and not optimized for pulse applications. The GTOs were tested as discharge switches in a low inductance circuit delivering 2ìs pulses with a maximum switching current of 1.4 kA (94.6 kA/cm2) and a current rise time of 2.4 kA/ìs. All the devices were switched until failure. The failure modes will be discussed.

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circuit was simulated in Pspice and the results indicated that the circuit inductance was ≈ 30 nH. A custom-built gate-drive circuit, which could deliver a peak current of 10 A, was connected between the gate and the anode. Note that this GTO requires a negative gate current (I_G) to be latched on and a positive I_G to be turned off. The devices were packaged in a TO-247 package.

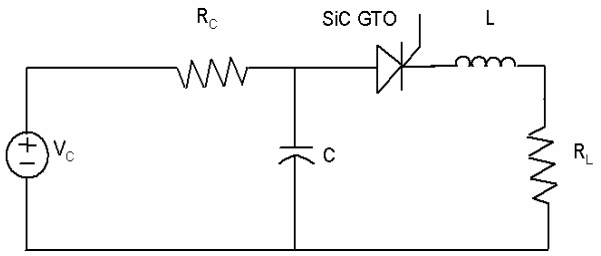

Figure 2. RLC ring down circuit

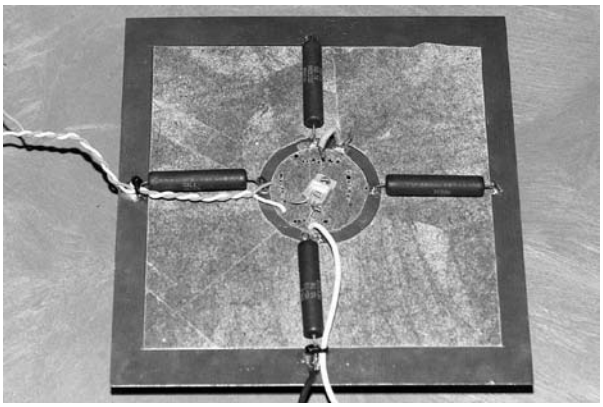

Figure 3. Top view of the switching fixture

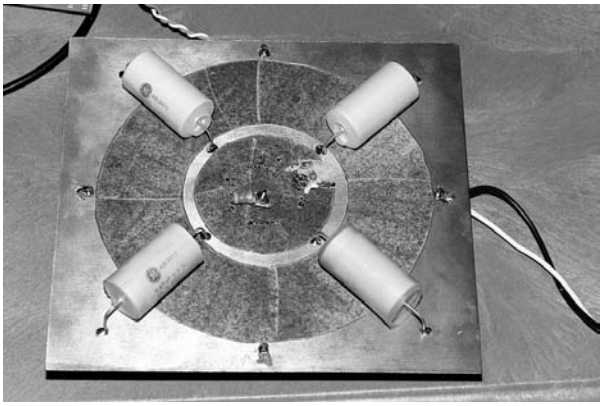

Figure 4. Bottom view of switching circuit

The anode was connected using 100, 1 mil gold wires and the gate used 14, 1 mil gold wires.

The devices were not connected to a heat sink; therefore, only low rep rate (time between shots greater than 3 s) stressing was done. After each 1000 shots, the devices were evaluated on the curve tracer and the gate turn-on, gate blocking, anode-to-cathode blocking, and the on-state resistance was examined. The device design was optimized for GTO operation and not high di/dt pulse stress performance. During the turn-on process large excess carrier plasma builds up in the vicinity of the gate region, which then spreads laterally across the device. If the anode current reaches its peak before the plasma spreads throughout the device then high-localized power dissipation and heating can damage the device. The plasma spreading time limits the di/dt of the device. The di/dt of the device can be improved by increasing the gate current at turn-on. For this experiment, the gate was turned on with a peak current of 8 A.

III. RESULTS AND DISCUSSION

Two SiC GTOs were used in the experiment. Device 1 was stressed at 100 V increments up to 700 V (1.4 kA). At the maximum voltage (700 V), device 1 was switched once before failure. Device 2 was stressed at V_{AC} of 400 V and I_C of 800 A for 1000 shots, then the device was stressed at 500V and 1kA for 2000 shots, and finally the device was stressed for 2 shots at 600 V and 1.2 kA at which time the device failed. Figure 5 shows a representative switching voltage and current waveforms at a peak cathode current I_C of 1.4 kA, full pulse width of 2 μs, di/dt of 2.36 kA/μs, and anode-to-cathode voltage of 700 V. The active area of the device is 37%, therefore, the maximum current density achieved was 94.6 kA/cm^2. As shown in figure 6, the peak power dissipated in the switch during the switching interval was 240 kW with a pulse width of 1 μs. At the peak current, the device was switched once before failure. High rep rate operation was not investigated at this time; however, follow on work will investigate high rep rate switching. Figure 7 shows the holding current as a function of the number of shots applied to the device. A small increase in holding current was observed from 0.22 A at a peak current of 800 A to 0.35 A at a peak current of 1.4 kA, however the forward voltage remained unchanged.

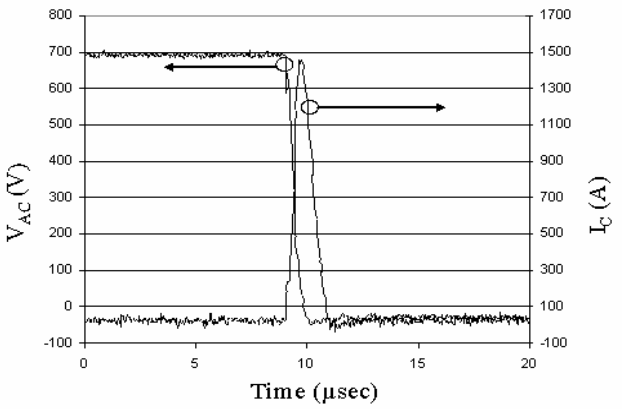

Figure 5. Voltage and current waveforms at 700 V and 1.4 kA

The blocking voltage V_{AC} was also investigated and the results showed no degradation of device anode-to-cathode blocking over the range of peak power. The forward conduction characteristics of the gate-to-anode diode did not change as the number of shots was increased.

However, as shown in figure 8, the reverse blocking of the gate-to-anode diode degraded with increased switching current.

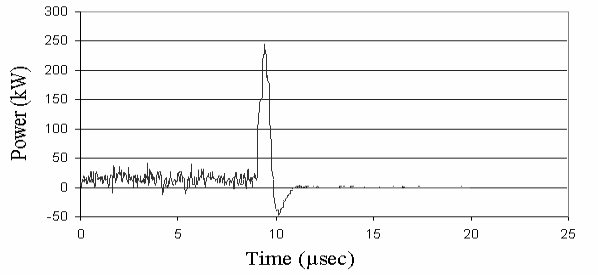

Figure 6. Peak power switched across the device

It can be seen in figure 8, trace D, that the leakage current is about 3 μA at a gate voltage of 15 V after the device was stressed at 400 V and 800 A for 1000 shots. Trace C shows a slight increase in leakage current to 5 μA after the device was stressed at 500 V and 1 kA for 1000 shots. The device was then stressed again at 500 V and 1 kA for 1000 additional shots as shown in Figure 8, trace B; the leakage current increased to 50 μA at 15 V which indicated that the junction was starting to be damaged. As shown in trace A in Figure 8, after the device was stressed at 1.2 kA for 2 shots, the leakage current in the gate was over 40 μA at a gate voltage of 5 V which rendered the device uncontrollable. The results indicated that the gate-to-anode junction was being damaged by the increasing high current stress (power dissipation) on the devices, which led to higher leakage current in the gate-to-anode junction. All the devices failed with high gate leakage when the gate was in reverse blocking. The failure was most likely caused by localized heating of the GTO at turn-on. For high di/dt switching, the current through the device is limited to a small turn-on area of the device around the gate, which increases the current density. The high-current density causes high power dissipation in the anode-gate area. The high - power dissipation in the gate causes damage to the passivation over the gate-to-anode oxide, which leads to the leakage current in the gate-to-anode junction.

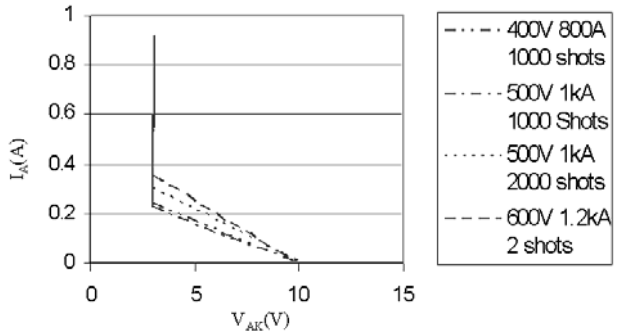

Figure 7. Holding current as a function of number of shots

Figure 9 shows a SEM image of a device after failure with the arrows pointing to the gate and anode fingers. The upper gold plate is the gate metallization, and the lower gold plate is the anode metallization. The SEM image shows that the damage to the device occurred around the gate-to-anode junction.

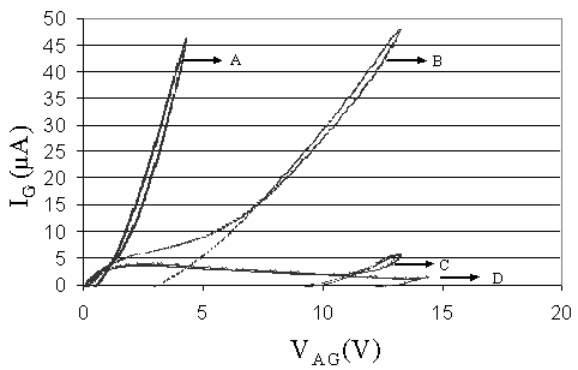

Figure 8. Reverse blocking of the gate-to-anode junction after failure

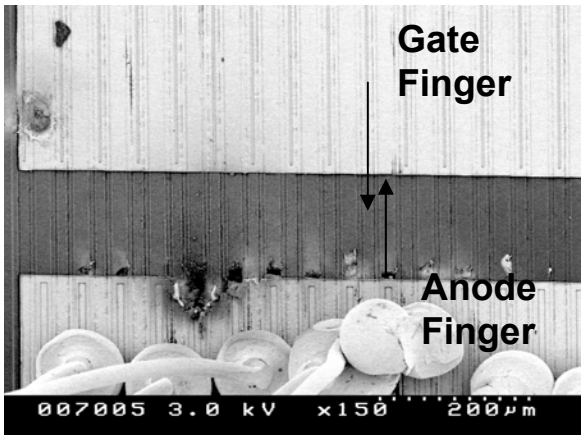

Figure 9. SEM image of device after failure

IV. CONCLUSION

The feasibility of the use of SiC GTOs for applications requiring fast rise time, narrow high pulses, was investigated. Although the devices used in this experiment were not optimized for turn-on, a peak current density of over 94.6 kA/cm^2 was reached. SEM was used to examine the devices after failure and the results indicated that the damage to the devices was on the anode fingers very close to the gate fingers. These results indicated that localized heating in the anode near the gate at turn-on most probably caused failure. The peak current and the number of shots can possibly be increased by optimizing the devices for turn-on.

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